

Entrepreneurial ID «venture leaders» 2007



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Structured Interconnects: we supply a revolutionary on-chip interconnection technology, the associated CAD tools, and design services to silicon vendors, allowing them to improve chip performance and power consumption while cutting on design time.

Industry: ICT

Biography

I was born in 1978 and I am completing the final year of the PhD program in Electronic Engineering at University of Bologna, Italy, in collaboration with the LSI, EPF Lausanne, Switzerland. During my PhD, I have published more than 20 international papers, some of which have been candidate for Best Paper Awards, and I have attended some of the leading conferences in digital design and digital automation. My fields of interest span across digital electronics, multiprocessor programming and nanotechnologies. I am fluent in English, French and Italian.

After spending several years in the academic environment, I am excited at the idea of turning my ideas into concrete products that people may enjoy using. During my research period, I have been trained to improve my:

- *teamwork and leadership of project teams*
- *ability to evaluate and choose among technical and strategic alternatives*
- *passion for innovation and openness to a rapidly changing environment*
- *dedication and commitment to meeting objectives and deadlines*
- *presentation and communication skills*

On the basis of these abilities, I am motivated to doing well in business environments, where matching customer demands and pushing for continued innovation is key.

Company / project

Structured Interconnects is aimed at serving the needs of silicon vendors. With the continued push for features and performance in today's chips, the System-on-Chip (SoC) paradigm, where multiple processing elements, memories and input/output devices are integrated into a single package, has emerged as a winner. Unfortunately, SoC design complexity is exponentially increasing, as the number of units integrated onto a single chip is doubling every 18 months. This trend creates a major bottleneck in the design of the on-chip interconnect, due to ever increasing bandwidth demands and more stringent physical constraints. This issue results in longer times to market and thus in unacceptable losses of sale opportunities for silicon vendors. As a consequence, there is a market for on-chip interconnection solution providers, which is currently estimated to be worth US\$ 150 million, increasing to US\$ 400 million by 2011.

Our start-up is aimed at providing a full solution to the interconnect design problem. On one hand, we have developed a radically new way of exchanging information on-chip, based on a packet-switching network paradigm (an on-chip version of the same principles driving the Internet). This approach, called Network-on-Chip (NoC), guarantees unlimited scalability to future designs of any complexity, while providing the means of cutting on design times. Compared to the competition, our solution is unique in that it simultaneously offers state-of-the-art technology (under the form of licensable IP cores), next-generation design tools, and the know-how to supply consulting services. Our target customers are the SoC vendors, such as Freescale, Samsung, STMicroelectronics and several others. Silicon vendors could use our technology to improve the performance, energy efficiency, and feature set of upcoming products, opening new exciting perspectives for millions of final users. For example, our technology may allow for personal communication devices with richer functionality yet longer battery life, unlock unprecedented levels of realism in gaming stations and virtual reality systems, and enable faster, more immersive Internet networking technology at the infrastructure level. We estimate that, by 2011, our company may reach the US\$ 90 million mark.

Structured Interconnects is currently in the incubation stage, with seed funding by EPF Lausanne. Our team is composed of seven academic experts in the field, three of which working on the project full-time. We have filed three patent applications and a prototype chip is due in Q2 2007. We are actively working to build up some business background, while simultaneously starting contacts with customers to establish the required credibility. We aim at incorporation towards the end of 2007, subject to acquiring VC funding (about US\$ 5 million in Round A) and the corresponding management guidance.